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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/776,834	02/11/2004	Alexander Burinskiy	100-24200 (P05758)	3018

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EXAMINER	
TON, MY TRANG	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 03/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/776,834	BURINSKIY ET AL.	
	Examiner	Art Unit	
	My-Trang N. Ton	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-14 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1,13 and 14 is/are rejected.

7)☒ Claim(s) 2-12 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 11 February 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

MY-TRANG NU TON
PRIMARY EXAMINER
02/28/05

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 02/11/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

Claim 14 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 14, the limitation "the first value turning off a first transistor and a second transistor, the logic high turn on a third transistor and a fourth transistor, the third transistor pulling down an output voltage on the output node, the fourth transistor pulling down an intermediate voltage on a second intermediate node to a second value, the second value turning on a fifth transistor that pulls down the output voltage on the output node" is misdescriptive of the present invention since such limitation is not seen as recited therein. In order to avoid any confusion, Applicant is required to particularly point out how these limitations read on the circuit arrangement of the drawings. Firstly, it appears that if considered M3 and M4 are the first and second transistors, and M5 and M6 are the third and fourth transistors, it is not seen to have "the first value turning off a first transistor and a second transistor" and "the logic high turn on a third transistor and a fourth transistor" as recited therein. And secondly, if considered M4 and M7 are the first and second transistors, and M3 and M8 are the third and fourth transistors, then the limitation "the third transistor pulling down an output voltage on the output node, the fourth transistor pulling down an intermediate voltage on a second intermediate node to

a second value, the second value turning on a fifth transistor that pulls down the output voltage on the output node" is lacking as recited therein.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by the prior art admitted by Applicant's Fig. 1.

The prior art, Fig. 1 discloses a level shifter including:

According to claim 1:

an inverter (M1, M2) having an input node (IN) and an intermediate node (an output node of M1 and M2), the input node (IN) having a logic state (HIGH or LOW), the intermediate node having a logic state (LOW or HIGH) opposite of the logic state of the input node (IN);

a first transistor (M4) that contacts the inverter (M1, M2) and a first output node (OUT), the first output node (OUT) having a logic state (HIGH or LOW);

a second transistor (M3) that contacts the inverter (M1, M2) and a second output node (OUT*), the second output node (OUT*) having a logic state (LOW or HIGH) opposite the logic state of the first output node (HIGH or LOW);

a third transistor (M6) that contacts the first transistor (M4) and the first output node (OUT); and

a fourth transistor (M5) that contacts the second transistor (M3) and the second output node (OUT*).

According to claim 13:

the inverter (M1, M2) is connected to a first supply voltage (VDD1), and the third and fourth transistors (M6 and M5) are connected to a second supply voltage (VDD2), the second supply voltage (VDD2) being greater than the first supply voltage (VDD1) (see the specification, pages 1-2, VDD1 = 1.2V, VDD2 = 3.6V).

Claim 1 is also rejected under 35 U.S.C. 102(b) as being anticipated by Taub (U.S Patent No. 6,385,099).

Taub discloses in Figs 2-3 a level shifter including:

According to claim 1:

an inverter (32) having an input node (Vint) and an intermediate node (34), the input node (Vint) having a logic state (HIGH or LOW), the intermediate node having a logic state (LOW or HIGH) opposite of the logic state of the input node (Vint);

a first transistor (28) that contacts the inverter (32) and a first output node (Vout2), the first output node (Vout2) having a logic state (HIGH or LOW);

a second transistor (30) that contacts the inverter (32) and a second output node (Vout1), the second output node (Vout1) having a logic state (LOW or HIGH) opposite the logic state of the first output node (HIGH or LOW);

a third transistor (24) that contacts the first transistor (28) and the first output node (Vout2); and

a fourth transistor (26) that contacts the second transistor (30) and the second output node (Vout1).

Claims 1 and 13 are also rejected under 35 U.S.C. 102(b) as being anticipated by Wang (U.S Patent No. 6,414,534).

Wang discloses in Figs. 1-2 a level shifting circuits including:

According to claim 1:

an inverter (MP1, MN1) having an input node (IN) and an intermediate node (INB), the input node (IN) having a logic state (HIGH or LOW), the intermediate node having a logic state (LOW or HIGH) opposite of the logic state of the input node (IN);

a first transistor (MN2) that contacts the inverter (MP1, MN1) and a first output node (OUTB), the first output node (OUTB) having a logic state (HIGH or LOW);

a second transistor (MN3) that contacts the inverter (MP1, MN1) and a second output node (OUT), the second output node (OUT) having a logic state (LOW or HIGH) opposite the logic state of the first output node (HIGH or LOW);

a third transistor (MP2) that contacts the first transistor (MN2) and the first output node (OUTB); and

a fourth transistor (MP3) that contacts the second transistor (MN3) and the second output node (OUT).

According to claim 13:

the inverter (MP1, MN1) is connected to a first supply voltage (VCCL), and the third and fourth transistors (MP2, MP3) are connected to a second supply voltage (VCCH), the second supply voltage (VCCH) being greater than the first supply voltage (VCCL) (see col. 5, lines 27-51).

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 and 13 are also rejected under 35 U.S.C. 102(e) as being anticipated by Shimada et al (U.S Patent No. 6,750,696).

Shimada et al disclose in fig. 1 a bias potential generation circuit including:

According to claim 1:

an inverter (2) having an input node (V1) and an intermediate node (V2), the input node (V1) having a logic state (HIGH or LOW), the intermediate node (V2) having a logic state (LOW or HIGH) opposite of the logic state of the input node (V1);

a first transistor (5) that contacts the inverter (2) and a first output node (V0), the first output node (V0) having a logic state (HIGH or LOW);

a second transistor (6) that contacts the inverter (2) and a second output node (/VO), the second output node (/VO) having a logic state (LOW or HIGH) opposite the logic state (HIGH or LOW) of the first output node (VO);

a third transistor (3) that contacts the first transistor (5) and the first output node (VO); and

a fourth transistor (4) that contacts the second transistor (6) and the second output node (/VO).

According to claim 13:

the inverter (2) is connected to a first supply voltage (VDD), and the third and fourth transistors (3, 4) are connected to a second supply voltage (VDDH), the second supply voltage (VDDH) being greater than the first supply voltage (VDD) (see col. 3, lines 44-45).

Claims 1 and 13 are also rejected under 35 U.S.C. 102(e) as being anticipated by Hayashi et al (U.S Patent No. 6,774,695).

Hayashi et al disclose in Fig. 1 a level conversion circuit including:

According to claim 1:

an inverter (Qp1, Qn1) having an input node (IN) and an intermediate node (IN*), the input node (IN) having a logic state (HIGH or LOW), the intermediate node (IN*) having a logic state (LOW or HIGH) opposite of the logic state of the input node (IN);

a first transistor (Qn2) that contacts the inverter (Qp1, Qn1) and a first output node (n1), the first output node (n1) having a logic state (HIGH or LOW);

a second transistor (Qn3) that contacts the inverter (Qp1, Qn1) and a second output node (n2), the second output node (n2) having a logic state (LOW or HIGH) opposite the logic state (HIGH or LOW) of the first output node (n1);

a third transistor (Qp2) that contacts the first transistor (Qn2) and the first output node (n1); and

a fourth transistor (Qp3) that contacts the second transistor (Qn3) and the second output node (n2).

According to claim 13:

the inverter (Qp1, Qn1) is connected to a first supply voltage (VDD), and the third and fourth transistors (Qp2, Qp3) are connected to a second supply voltage (VDD2), the second supply voltage (VDD2) being greater than the first supply voltage (VDD) (see col. 3, lines 44-45) (see col. 8, lines 45-50, VDD = 1.5V, VDD2 = 3.3V).

Claims 1 and 13 are rejected under 35 U.S.C. 102(e) as being anticipated by Aoki (U.S Patent No. 6,717,453).

Aoki discloses in Figs 1-11 a level shift circuit including:

According to claim 1:

an inverter (P2, N2) having an input node (an output of P1, N1) and an intermediate node (an output node of P2, N2), the input node having a logic state (HIGH or LOW), the intermediate node having a logic state (LOW or HIGH) opposite of the logic state of the input node;

a first transistor (N3) that contacts the inverter (N2, P2) and a first output node (14), the first output node (14) having a logic state (HIGH or LOW);

a second transistor (N4) that contacts the inverter (N2, P2) and a second output node (15), the second output node (15) having a logic state (LOW or HIGH) opposite the logic state of the first output node (HIGH or LOW);

a third transistor (P3) that contacts the first transistor (N3) and the first output node (14); and

a fourth transistor (P4) that contacts the second transistor (N4) and the second output node (15).

According to claim 13:

the inverter (N2, P2) is connected to a first supply voltage (VDD1), and the third and fourth transistors (P3, P4) are connected to a second supply voltage (VDD2), the second supply voltage (VDD2) being greater than the first supply voltage (VDD1) (see col. 8, line 9).

Claim 1 is also rejected under 35 U.S.C. 102(e) as being anticipated by Ziesler et al (U.S Patent No. 6,777,992).

Ziesler et al disclose in fig. 1 a flip-flop circuit including:

According to claim 1:

an inverter (24b) having an input node (22) and an intermediate node (an output of 24b), the input node (22) having a logic state (HIGH or LOW), the intermediate node (the output of 24b) having a logic state (LOW or HIGH) opposite of the logic state of the input node (22);

a first transistor (26a) that contacts the inverter (24b) and a first output node (X), the first output node (X) having a logic state (HIGH or LOW);

a second transistor (26b) that contacts the inverter (24b) and a second output node (Y), the second output node (Y) having a logic state (LOW or HIGH) opposite the logic state (HIGH or LOW) of the first output node (X);

a third transistor (20a) that contacts the first transistor (26a) and the first output node (X); and

a fourth transistor (20b) that contacts the second transistor (26b) and the second output node (Y).

Allowable Subject Matter

Claims 2-12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art disclosed or suggested to show the particular structure and/or the particular operation recited in these claims namely: "a seventh transistor" in combination with "a fifth transistor" and "a sixth transistor" as recited in claim 2.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to My-Trang N. Ton whose telephone number is 571-272-1754. The examiner can normally be reached on 7:00 a.m - 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

My-Trang N. Ton
Primary Examiner
Art Unit 2816

February 28, 2005